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Envision, Enable, and Empower  
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## FORMAL EQUIVALENCE VERIFICATION BETWEEN RTL/GATE-LEVEL NETLIST AND FPGA FULL-CHIP NETLIST USING CADENCE CONFORMAL LOGIC EQUIVALENCE CHECKER

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### ABSTRACT

Formal Equivalence Verification (FEV) nowadays has emerged as a method in FPGA design flow. However, FPGA designers didn't give that much of importance of doing FEV on full-chip level. Unlike ASIC, the full chip of FPGA doesn't have any resemblance on a RTL code or Gate-level netlist unless a bitstream (generated via a synthesis tool) is loaded on it. Another reason is that most of the FEV tools are specifically used for ASIC design though some FPGA designers used FEV but not on performing logic equivalence between RTL/Gate-level netlist versus FPGA full-chip netlist.

This paper designs a working process flow and discusses pitfalls encountered along the way. The researcher successfully performs Formal Equivalence Verification between RTL/Gate-level netlist and full chip FPGA using Conformal, a Cadence Logic Equivalence Checking Tool. This study will lay the foundation of performing Formal Equivalence Verification between RTL/Gate-level netlist and FPGA full-chip netlist. Since FEV exhaustively checks for errors and bugs, for future use it may help FPGA designers increase their design efficiency.

**Keywords:** Formal Equivalence Verification, FPGA, Full-chip FEV, Logic Equivalence Checker.

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